

What Is Claimed Is:

Sub B' / 5

1. A high electron mobility transistor using a Group III-V compound semiconductor, comprising

an undoped second channel layer laminated on an InP substrate via a buffer layer;

an undoped first channel layer laminated on said second channel layer; and

a doped electron-supplying layer laminated on

10 said first channel layer,

wherein said first channel layer is composed of  $\text{In}_{1-x}\text{Ga}_x\text{As}$  and has an energy level of conduction band lower than that of said electron-supplying layer,

said second channel layer is composed of a Group

15 III-V compound semiconductor using a Group V element other than P, has an energy level of conduction band higher than that of the first channel layer, and has a band gap wider than that of the first channel layer.

Sub C' / 20

2. The high electron mobility transistor as described in claim 1, wherein said first and second channel layers are formed to have a thickness small enough to have discrete quantum levels, a first quantum level being formed only in the first channel layer, and a second

25 quantum level being formed in both the first and second channel layers.

Sub B2  
3. The high electron mobility transistor as described in claim 1 or claim 2, wherein said electron-supplying layer is composed of  $\text{In}_{1-y}\text{Al}_y\text{As}$ , the first channel layer is composed of  $\text{In}_{1-x}\text{Ga}_x\text{As}$ , and the second channel layer is composed of  $\text{In}_{1-x}(\text{Al}_{1-z}\text{Ga}_z)_x\text{As}$ .

4. The high electron mobility transistor as described in claim 1 or claim 2, wherein said electron-supplying layer is composed of  $\text{In}_{1-y}\text{Al}_y\text{As}$ , the first channel layer is composed of  $\text{In}_{1-x}\text{Ga}_x\text{As}$ , and the second channel layer is composed of  $\text{In}_{1-x}(\text{Al}_{1-z}\text{Ga}_z)_x(\text{As}_{1-z_2}\text{Sb}_{z_2})$ .

Sub A1  
5. The high electron mobility transistor as described in claim 3 or claim 4, wherein the thickness of said first channel layer is 3-7 nm.

6. The high electron mobility transistor as described in claim 3 or claim 4, wherein the thickness of said second channel layer is 10-20 nm.

7. The high electron mobility transistor as described in claim 3 or claim 4, wherein the composition ratio (1-z) of Al element in said second channel layer is 0.05-0.5.

Sub B3  
8. The high electron mobility transistor as described in claim 1 or claim 2, wherein said electron-

supplying layer is composed of  $\text{In}_{1-y}\text{Al}_y\text{As}$ , the first channel layer is composed of  $\text{In}_{1-x}\text{Ga}_x\text{As}$ , and the second channel layer is composed of  $\text{In}_{1-x}\text{Ga}_x\text{As}$  with the In composition ratio lower and the gallium composition ratio higher than those in the first channel layer.

9. The high electron mobility transistor as described in claim 1 or claim 2, wherein an element separation groove is formed which extends from said electron-supplying layer to said buffer layer.

10. A high electron mobility transistor using a Group III-V compound semiconductor, comprising an undoped second channel layer laminated on an InP substrate via a buffer layer and composed of  $\text{In}_{1-x}(\text{Al}_{1-z}\text{Ga}_z)_x\text{As}$  (where the composition ratio  $(z-1)$  of Al is 0.05~0.5) which is lattice matched to InP, an undoped first channel layer laminated on said second channel layer and composed of  $\text{In}_{1-x}\text{Ga}_x\text{As}$  which is lattice matched to InP, and a doped electron-supplying layer laminated on said first channel layer and composed of  $\text{In}_{1-y}\text{Al}_y\text{As}$  which is lattice matched to InP.

11. The high electron mobility transistor as described in claim 10, wherein said first and second channel layers are formed to have a thickness small enough

to have the discrete quantum levels, a first quantum level being formed only in the first channel layer, and a second quantum level being formed in both the first and second channel layers.

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